DESCRIPTION

RECORDING CLOCK GENERATION APPARATUS

TECHNICAL FIELD

The present invention relates to a recording clock generation apparatus and, more particularly, to sharing of a wobble PLL circuit and a physical address data decoding circuit in an apparatus adaptable to both of DVD-R/RW recording and +RW/+R recording.

BACKGROUND ART

A conventional DVD-R/RW and +RW/+R recorder is constituted as shown in figure 6. This apparatus is provided with both of a 186-multiply wobble PLL circuit and a 32-multiply wobble PLL circuit. Usually, address information, additional information, and a sync signal are recorded on these types of recording media to specify recording positions (tracks) on optical discs even when no data are recorded on the optical discs. As a method for modulating the above-mentioned address information and additional information, a format called "Land Pre-pit" (hereinafter also referred to as "LPP") is employed for the DVD-R/RW while a format called "Address In Pre-groove" (hereinafter also referred to as "ADIP") is employed for the +RW/+R.

In the figure, reference numeral 601 denotes a wobble signal,

which is input to a time domain filter 602 for noise removal. The signal from which noise is removed by the time domain filter 602 is input to a subsequent wobble period averaging circuit 603, wherein variations in the cycle of the signal are averaged.

A phase correction circuit 614 performs phase compensation by correcting a timing error in the recorded data with respect to the ADIP signal, which timing error is caused by that the cycle of the ADIP signal is converted, and either the LPP signal or the ADIP signal outputted through a timing conversion circuit 616 is selected by a selector 615 to be input to the phase compensation circuit 614.

A phase comparator 604 compares the phase of the output from the wobble period averaging circuit 603 with the phase of the output from a selector 612. Reference numeral 605 denotes a charge pump for digital-to-analog converting the output of the phase comparator 604 in order to control a VCO (Voltage-Controlled Oscillator) which is a subsequent analog circuit. Reference numeral 606 denotes a selector for supplying the output of the charge pump 605 to either of a VCO (Voltage-Controlled Oscillator) 607 or a VCO 608.

Reference numeral 609 denotes a selector for selecting either the output of the VOC 607 or the output of the VOC 608, and supplying the selected signal to an arithmetic circuit 613 described later, 610 denotes a 1/186 frequency divider, 611 denotes a 1/32 frequency divider, and 612 denotes a selector for

selecting either the output of the 1/186 frequency divider 610 or the output of the 1/32 frequency divider 611, and outputting the selected signal. Further, reference numeral 613 denotes an arithmetic circuit for performing frequency-division of a reference clock, detection of PLL lock/unlock, detection of frequency error, detection of phase inversion, and the like.

Further, reference numeral 617 denotes an LPP decoder for decoding a binarized LPP signal to output address data, and 618 denotes an ADIP decoder for decoding a binarized ADIP signal to output address data. Further, reference numeral 691 denotes a selector for selecting either the output of the LPP decoder 617 or the output of the ADIP decoder 618, and outputting the selected signal as address data.

In the above-mentioned construction, when the input signal is a land pre-pit signal based on the DVD-R/R standard, the selector 606 outputs the input signal to the VCO (607), and the output of the 1/186 frequency-divider 610 is selected by the selector 612 to be output to the phase comparator 604, and further, a deviation from the reference clock is calculated by the arithmetic circuit 613, thereby outputting a signal WPLLOK 615 indicating that the PLL circuit is locked, and a recording clock frequency OK signal WREFOK 616.

As described above, there is a multi-optical-disc-compatible recorder which can perform recording and playback in/from the above-mentioned plural optical discs by providing a means for

converting address information that is detected from the binarized wobble signal based on the +RW/+R standard into a land pre-pit signal based on the DVD-R/RW standard (for example, refer to Japanese Published Patent Application No.2003-100015 and Japanese Published Patent Application No.2003-123257). This apparatus detects the address information from the binarized wobble signal, and converts the address information which also concerns the cycle of the binarized wobble signal into a land pre-pit signal based on the DVD-R/RW standard, thereby realizing cycle protection between the two sync signals to avoid destruction of the recorded data due to recording of data into a wrong position on the disc.

The recording clock generation apparatus of the conventional DVD-R/RW and +RW/+R recorder is constructed as described above, and contains the PLL circuits corresponding to the formats of the DVD-R/RW standard and the +RW/+R standard, respectively. Therefore, the circuit scale of the apparatus is undesirably increased, which is disadvantageous in terms of cost.

Further, the means for converting the binarized wobble signal based on the +RW/+R standard into the land pre-pit signal based on the DVD-R/RW standard, which is aimed at sync protection, complicates the structure of the conversion circuit.

The present invention is made to solve the above-mentioned problems and has for its object to provide a recording clock generation apparatus to be used in a DVD-R/RW and +RW/+R recorder,

which is compatible to the respective formats of the DVD-R/RW standard and the +RW/+R standard, and avoids an increase in the circuit scale.

DISCLOSURE OF THE INVENTION

According to the present invention (Claim 1), there is provided a recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording using the same recorder, and the apparatus comprises a frequency conversion circuit for converting an inputted 32T-cycle binarized wobble signal based on a +RW/+R standard into a 186T-cycle binarized wobble signal based on a DVD-R/RW standard; a selector for selecting either the converted 186T-cycle binarized wobble signal that is outputted from the frequency conversion circuit or the inputted 186T-cycle binarized wobble signal, and outputting the selected signal; and a PLL circuit for 186-multiplying the binarized wobble signal on receipt of the output of the selector.

According to the present invention (Claim 2), there is provided a recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording using the same recorder, and the apparatus comprises a frequency conversion circuit for converting an inputted 186T-cycle binarized wobble signal based on a DVD-R/RW standard into a 32T-

cycle binarized wobble signal based on a +RW/+R standard; a selector for selecting either the converted 32T-cycle binarized wobble signal that is outputted from the frequency conversion circuit or the inputted 32T-cycle binarized wobble signal, and outputting the selected signal; and a PLL circuit for 32-multiplying the binarized wobble signal on receipt of the output of the selector.

According to the present invention (Claim 3), the recording clock generation apparatus defined in Claim 1 further includes a physical address data decoder comprising a circuit for converting a binarized ADIP signal based on the +RW/+R standard into a binarized land pre-pit signal based on the DVD-R/RW standard, and a circuit for detecting even sync data, odd sync data, 0 data, and 1 data from the binarized land pre-pit signal.

According to the present invention (Claim 4), the recording clock generation apparatus defined in Claim 2 further includes a physical address data decoder comprising a circuit for converting a binarized land pre-pit signal based on the DVD-R/RW standard into a binarized ADIP signal based on the +RW/+R standard, and a circuit for detecting sync data, 0 data, and 1 data from the binarized ADIP signal.

According to the present invention (Claim 5), the recording clock generation apparatus defined in Claim 1 further includes a circuit for converting a binarized ADIP signal based on the +RW/+R standard into a binarized land pre-pit signal based on the

DVD-R/RW standard; and a phase adjustment circuit for performing phase adjustment between the 186T-cycle binarized wobble signal and the binarized land pre-pit signal which are based on the DVD-R/RW standard.

According to the present invention (Claim 6), the recording clock generation apparatus defined in Claim 2 further includes a circuit for converting a binarized land pre-pit signal based on the DVD-R/RW standard into a binarized ADIP signal based on +RW/+R standard; and a phase adjustment circuit for performing phase adjustment between the 32T-cycle binarized wobble signal and the binarized ADIP signal which are based on the +RW/+R standard.

According to the present invention (Claim 7), there is provided a recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording using the same recorder, and the apparatus comprises a frequency conversion circuit for converting an inputted first cycle binarized wobble signal based on a first standard into a second cycle binarized wobble signal based on a second standard; a selector for selecting either the second cycle binarized wobble signal that is outputted from the frequency conversion circuit or the inputted first cycle binarized wobble signal, and outputting the selected signal; and a PLL circuit for multiplying the binarized wobble signal to change its cycle from the wobble cycle

to the cycle of the recording clock, on receipt of the output of the selector.

According to the present invention (Claim 1), a recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording using the same recorder, comprises a frequency conversion circuit for converting an inputted 32T-cycle binarized wobble signal based on a +RW/+R standard into a 186T-cycle binarized wobble signal based on a DVD-R/RW standard; a selector for selecting either the converted 186T-cycle binarized wobble signal that is outputted from the frequency conversion circuit or the inputted 186T-cycle binarized wobble signal, and outputting the selected signal; and a PLL circuit for 186-multiplying the binarized wobble signal on receipt of the output of the selector. Therefore, circuits in subsequent stages can be shared by inputting, to the subsequent circuits, the converted 186T-cycle binarized wobble signal during DVD-R/RW recording and the 186T-cycle binarized wobble signal during +RW/+R recording, resulting in reductions in circuit scale and production cost.

Further, according to the present invention (Claim 2), a recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording using the same recorder, comprises a frequency conversion circuit for converting

an inputted 186T-cycle binarized wobble signal based on a DVD-R/RW standard into a 32T-cycle binarized wobble signal based on a +RW/+R standard; a selector for selecting either the converted 32T-cycle binarized wobble signal that is outputted from the frequency conversion circuit or the inputted 32T-cycle binarized wobble signal, and outputting the selected signal; and a PLL circuit for 32-multiplying the binarized wobble signal on receipt of the output of the selector. Therefore, circuits in subsequent stages can be shared by inputting, to the subsequent circuits, the converted 32T-cycle binarized wobble signal during DVD-R/RW recording and the 32T-cycle binarized wobble signal during +RW/+R recording, resulting in reductions in circuit scale and production cost.

Further, according to the present invention (Claim 3), the recording clock generation apparatus defined in Claim 1 includes a physical address data decoder comprising a circuit for converting a binarized ADIP signal based on the +RW/+R standard into a binarized land pre-pit signal based on the DVD-R/RW standard, and a circuit for detecting even sync data, odd sync data, 0 data, and 1 data from the binarized land pre-pit signal. Therefore, subsequent circuits from an LPP decoding circuit can be shared by inputting, to the subsequent circuits, the converted binarized land pre-pit signal during +RW/+R recording and the binarized land pre-pit signal during DVD-R/RW recording. Further, since the data of the binarized ADIP signal is converted directly

into the binarized land pre-pit signal, the conversion circuit is not complicated, resulting in reductions in circuit scale and production cost.

Further, according to the present invention (Claim 4), the recording clock generation apparatus defined in Claim 2 includes a physical address data decoder comprising a circuit for converting a binarized land pre-pit signal based on the DVD-R/RW standard into a binarized ADIP signal based on the +RW/+R standard, and a circuit for detecting sync data, 0 data, and 1 data from the binarized ADIP signal. Therefore, subsequent circuits from an ADIP decoding circuit can be shared by inputting, to the subsequent circuits, the converted binarized land pre-pit signal during DVD-R/RW recording and the binarized land pre-pit signal during +RW/+R recording. Further, since the data of the binarized LPP signal is converted directly into the binarized ADIP signal, the conversion circuit is not complicated, resulting in reductions in circuit scale and production cost.

Further, according to the present invention (Claim 5), the recording clock generation apparatus defined in Claim 1 includes a circuit for converting a binarized ADIP signal based on the +RW/+R standard into a binarized land pre-pit signal based on the DVD-R/RW standard; and a phase adjustment circuit for performing phase adjustment between the 186T-cycle binarized wobble signal and the binarized land pre-pit signal which are based on the DVD-R/RW standard. Therefore, the position adjustment circuit for

the recorded data and the binarized land pre-pit signal can be shared by performing phase compensation by correcting a timing error in the recorded data with respect to the land pre-pit signal due to conversion of the cycle thereof, resulting in a reduction in circuit scale.

Further, according to the present invention (Claim 6), the recording clock generation apparatus defined in Claim 2 includes a circuit for converting a binarized land pre-pit signal based on the DVD-R/RW standard into a binarized ADIP signal based on +RW/+R standard; and a phase adjustment circuit for performing phase adjustment between the 32T-cycle binarized wobble signal and the binarized ADIP signal which are based on the +RW/+R standard. Therefore, the position adjustment circuit for the recorded data and the binarized ADIP signal can be shared by performing phase compensation by correcting a timing error in the recorded data with respect to the ADIP signal due to conversion of the cycle thereof, resulting in a reduction in circuit scale.

Further, according to the present invention (Claim 7), a recording clock generation apparatus for generating a recording clock to be used when performing recording on plural media based on different standards of frequencies at recording using the same recorder, comprises a frequency conversion circuit for converting an inputted first cycle binarized wobble signal based on a first standard into a second cycle binarized wobble signal based on a second standard; a selector for selecting either the second cycle

binarized wobble signal that is outputted from the frequency conversion circuit or the inputted first cycle binarized wobble signal, and outputting the selected signal; and a PLL circuit for multiplying the binarized wobble signal to change its cycle from the wobble cycle to the cycle of the recording clock, on receipt of the output of the selector. Therefore, circuits in subsequent stages can be shared by inputting, for example, a converted 186T-cycle binarized wobble signal during DVD-R/RW recording while inputting a 186T-cycle binarized wobble signal during +RW/+R recording, to the subsequent circuits, resulting in reductions in circuit scale and production cost.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram illustrating a recording clock generation apparatus according to a first embodiment of the present invention.

Figure 2 is a diagram illustrating waveforms of a conversion circuit from a 32T-cycle binarized wobble signal to a 186T-cycle binarized wobble signal, which signals are shown in figure 1.

Figure 3 is a diagram illustrating waveforms of a conversion circuit from an ADIP signal to a land pre-pit signal, which signals are shown in figure 1.

Figure 4 is a diagram illustrating waveforms of phase correction shown in figure 1.

Figure 5 is a diagram illustrating waveforms of position

adjustment between recorded data of a DVD recorder and a land pre-pit signal.

Figure 6 is a block diagram illustrating the construction of the conventional recording clock generation apparatus.

Figure 7 is a block diagram illustrating a modification of a recording clock generation apparatus according to the first embodiment.

Figure 8(a) is a block diagram illustrating the specific construction of a 32T→186T conversion circuit 106, and figure 8(b) is a diagram illustrating clock waveforms in the respective components of the circuit shown in figure 8(a).

BEST MODE TO EXECUTE THE INVENTION

(Embodiment 1)

Hereinafter, a recording clock generation apparatus used in a DVD-R/RW or +RW/+R recorder according to a first embodiment of the present invention will be described with reference to the drawings.

With reference to figure 1, 104 denotes a time domain filter for removing noise from an inputted binarized signal; 105 denotes a wobble cycle averaging circuit for averaging the cycle of the binarized signal outputted from the time domain filter 104; 106 denotes a 32T→186T conversion circuit for converting the output of the wobble cycle averaging circuit 105 into a 186T-cycle binarized wobble signal; 108 denotes a selector for selecting

either the output of the wobble cycle averaging circuit 105 or the output of the 32T→186T conversion circuit 106, and outputting the selected signal; and 110 denotes a phase correction circuit for correcting the phase of the binarized wobble signal outputted from the selector 108.

Further, 111 denotes a phase comparator for comparing the phase of the output of the phase correction circuit 110 with the phase of the output signal of a 1/186 frequency divider 114 which is described later; 112 denotes a charge pump for digital-to-analog converting the output of the phase comparator 111 to control a 186 frequency multiply VCO (Voltage Controlled Oscillator) as a subsequent analog circuit; 114 denotes a 1/186 frequency divider for reconstructing a 186-multiplied output 1T cycle recording clock WTCK 117; and 115 denotes an arithmetic circuit for performing processings such as division of a reference clock, detection of PLL lock/unlock, detection of frequency error, and detection of phase inversion.

Furthermore, 102 denotes a binarized land pre-pit signal to be used during DVD-R/RW recording; 103 denotes a binarized ADIP (address in pre-groove) signal to be used during +RW/+R recording; 107 denotes an ADIP→LPP conversion circuit for converting the binarized ADIP signal 103 into a binarized land pre-pit signal; 109 denotes a selector for selecting either the binarized LPP signal 102 or the converted binarized LPP signal outputted from the ADIP→LPP conversion circuit 107, and

outputting the selected signal; and 116 denotes an LPP decoder for decoding the binarized LPP signal outputted from the selector 109, and outputting the decoded signal as address data 120. The address data 120 include even sync data, odd sync data, 0 data and 1 data.

Next, the operation will be described. Since the fundamental operation as a PLL circuit is identical to that of the conventional apparatus, only the characteristic operation of the present invention will be mainly described hereinafter. A 186T-cycle binarized wobble signal is inputted as an input wobble 101 during DVD-R/RW recording, while a 32T-cycle binarized wobble signal is inputted as an input wobble 101 during +RW/+R recording. The selector 108 selects the output of the wobble cycle averaging circuit 105 during DVD-R/RW recording based on the LPP format standard, and the selector 108 selects the output of the circuit 106 which converts the 32T-cycle binarized wobble signal into the 186T-cycle binarized wobble signal during +RW/+R recording based on the ADIP format standard, thereby sharing the subsequent PLL circuits (111~116).

In this first embodiment, only a single system comprising a VCO and a frequency divider for DVD-R/RW is adaptable to different formats. The circuit 106 for converting a 32T-cycle binarized wobble signal into a 186T-cycle binarized wobble signal converts, as shown in figure 2, a 32T-cycle binarized wobble signal 201 into a 186T-cycle binarized wobble signal 202.

Figure 8(a) is a block diagram illustrating the specific construction of the 32T→186T conversion circuit 106. Further, figure 8(b) is a diagram illustrating clock waveforms at the respective parts of the circuit shown in figure 8(a).

A clock of 36T shown in the uppermost line of figure 8(b) passes through a counter 1060 and a comparator 1061 to be outputted as a timing waveform indicating the number of 32T wobbles (integer parts) obtained when converting the clock from 32T to 186T as shown in the second line. Since 32T multiplied by 5.8125 is 186T, a rising timing of 186T occurs during a period from the [5.8125×n]th 32T to the ([5.8125×n]+1)th 32T ([] is a Gauss notation indicating a decimal cut-off value, and n is a positive integer).

Further, the third line of figure 8(b) shows an output waveform of the 32T wobble signal which has passed through a cycle measurement unit 1062 and a fraction component timing unit 1063, and the timing is delayed by a length (5.8125×n-[5.8125×n]) times as long as the cycle of the 32T wobble signal during a period from the [5.8125×n]th integer part to the ([5.8125×n]+1)th integer part of the 32T wobble signal in the first line.

The lowermost line of figure 8(b) shows a 186T signal outputted from a waveform generator 1065 after the output of the comparator 1061 and the output of the fraction component timing unit 1063 are ORed (AND circuit 1064).

In figure 1, the binarized land pre-pit signal 102 is

supplied during DVD-R/RW recording while the binarized ADIP signal 103 is supplied during +RW/+R recording. The selector 109 selects the binarized land pre-pit signal 102 during the DVD-R/RW recording, and selects the converted binarized land pre-pit signal 102 that is obtained by converting the binarized ADIP signal thereto during the +RW/+R recording, whereby the land pre-pit decoder 116 and the following circuits can be shared. However, processing such as error correction of the address data 120 to be performed during the DVD-R/RW recording is different from that to be performed during the RW/+R recording. The ADIP→LPP circuit 107 for converting a binarized ADIP signal into a binarized land pre-pit signal performs conversion of an ADIP sync signal 302 into a land pre-pit sync even position signal 303 shown in figure 3, conversion of an ADIP 0 signal 304 into a land pre-pit 0 signal 305 shown in figure 3, and conversion of an ADIP 1 signal 306 into a land pre-pit 1 signal 307 shown in figure 3.

Further, since the selectors 108 and 109 perform selection of output signals as described above during the DVD-R/RW or +RW/+R recording, the phase correction circuit 110 can be shared.

The binarized wobble signal 101 which has passed through the time domain filter 104 and the wobble cycle averaging circuit 106 has a propagation delay with respect to the land pre-pit signal 102, and the phase correction circuit 110 performs phase adjustment on the 186T-cycle binarized wobble signal 401 and the binarized land pre-pit signal 402 shown in figure 4. Further,

the phase adjustment is carried out so that the time t403 becomes equal to the time t404.

Further, a description will be given of the output waveform of the phase correction circuit 110 when the above-mentioned recording clock generation apparatus is incorporated in a DVD recorder. With reference to figure 5, a binarized land pre-pit signal 502 is a binarized land pre-pit signal during the DVD-R/RW recording while it is a signal obtained by converting the binarized ADIP signal thereto during the +RW/+R recording. Position adjustment of the binarized land pre-pit signal 502 is carried out by adjusting the position of the recorded data 501 according to the position of the binarized land pre-pit signal 502.

As described above, the recording clock generation apparatus of the DVD-R/RW and +RW/+R recorder according to the first embodiment is provided with the circuit 106 for converting a 32T-cycle binarized wobble signal based on the +RW/+R standard into a 186T-cycle binarized wobble signal based on the DVD-R/RW standard. As for the 32T-cycle binarized wobble signal, it is converted into a 186T-cycle binarized wobble signal and then inputted to the subsequent 186 frequency multiply wobble PLL circuit. Therefore, the components corresponding to the 32 frequency multiply wobble PLL circuit are dispensed with in the PLL circuit, and thereby the VCO that occupies a large area is deleted, resulting in a recorder which can deal with media corresponding

to the two standards of DVD-R/RW and +RW/+R by sharing the 186 frequency multiply wobble PLL circuit based on the DVD-R/RW standard.

Further, the recording clock generation apparatus is provided with the ADIP→LPP conversion circuit 107 and the selector 109, and the converted binarized land pre-pit signal is inputted to the subsequent circuits from the LPP decoding circuit during the +RW/+R recording while the binarized land pre-pit signal is inputted thereto during the DVD-R/RW recording, and therefore, the subsequent circuits from the LPP decoding circuit can be shared. Further, since the data of the binarized ADIP signal is converted directly into the binarized land pre-pit signal, the conversion circuit is not complicated, resulting in reduced circuit area and reduced production cost.

Furthermore, since the output of the ADIP→LPP conversion circuit 107 is input to the phase correction circuit 110, the position adjustment circuit for the recorded data and the binarized land pre-pit signal can be shared, resulting in reduced circuit scale.

In the above-mentioned embodiment, the PLL circuit for the DVD-R/RW standard is shared by converting the 32T-cycle binarized wobble signal based on the +RW/+R standard into the 186T-cycle binarized wobble signal based on the DVD-R/RW standard, whereby the 32 frequency multiply wobble PLL circuit for the +RW/+R standard can be dispensed with. However, the recording clock

generation apparatus may be constructed as shown in figure 7. That is, a 186T→32T conversion circuit 701 for converting a 186T-cycle binarized wobble signal based on the DVD-R/RW standard into a 32T-cycle binarized wobble signal based on the DVD+R/+RW standard is provided, a 1/32 frequency-division circuit 702 and a VCO (32-multiply) 703 are provided as the subsequent PLL circuits, and further, an LPP→ADIP conversion circuit 704 is provided instead of the ADIP→LPP conversion circuit 107 and an ADIP decoder 705 is provided instead of the LPP decoder 116, whereby the PLL circuits for the DVD+R/+R standard are shared, and the 186 frequency multiply wobble PLL circuit for the DVD-R/-RW standard can be dispensed with.

In this case, the phase correction circuit 110 performs phase compensation by correcting a timing error in the recorded data with respect to the ADIP signal, which is caused by that the cycle of the ADIP signal is converted. Further, sync data, 0 data, and 1 data are included as address data 120 outputted from the ADIP decoder 705.

APPLICABILITY IN INDUSTRY

A recording clock generation apparatus according to the present invention is useful for such as a system LSI for a DVD-R/RW and +RW/+R recording drive for PCs, having a DVD-R/RW and +RW/+R recorder. Further, it is also applicable to such as a system LSI for a DVD-R/RW and +RW/+R recorder for consumer use.